SIGMA-DELTA MODULATION INVERTER WITH PROGRAMMABLE WAVEFORM OUTPUT

FIELD OF THE INVENTION

[0001]   The present invention relates to an inverter for converting a DC input voltage into an AC output voltage using the sigma-delta modulation (SDM).   More specifically, this invention relates to a sigma-delta modulation (SDM) DC/AC inverter with programmable waveform output.

BACKGROUND OF THE INVENTION

[0002]   The DC/AC inverter has been the major essentials for implementing the uninterrupted power supply (UPS), AC power sources, and any kind of the AC motor drivers etc.   Due to the rapid progress in the development of the power electronics, many approaches for realizing a compact inverter with high efficiency have been proposed.

[0003]   In year 1988, the phase-controlled DC/AC Inverter has been proposed for using the differences of phase angles between different switches to modulate the output voltage.   The above-mentioned phase-controlled DC/AC Inverter has relatively a simpler configuration, a higher power efficiency, a minimized volume of the isolation transformer due to the high-frequency switching so as to be beneficial to the manufacturing costs and the space limitations.   However, the total harmonic distortions (THD) of the output voltages of this kind of inverters are relatively larger.

[0004]   Nowadays, the widely used control strategies for realizing a DC/AC inverter is the pulse width modulation (PWM) for using an input

reference signal to compare with a triangular waveform so as to produce a width-modulated pulse to fulfill the object of controlling output voltage waveforms. In general, a voltage source inverter will have an output voltage of a rectangular waveform with a higher harmonic so as to decrease the power efficiency, therefore, the PWM inverter circuits can be employed to solve the problems regarding the voltage modulations and the waveforms distortions. The PWM is mainly focused on the control of the on/off of the power switches of the inverter circuits so as to get a series of pulses with equivalent-amplitudes but with nonequivalent-widths thus the widths of the pulses will form a sinusoidal distribution according to the Fourier series and the combinations of the pulses will form an equivalent sinusoidal voltage waveforms so as to engage in the modulation of each pulse in accordance with certain rules to change the magnitudes of the output voltages as well as the frequencies.

[0005]   Due to the triangular waves are employed to compare with the reference signals in the above-mentioned PWM, it is not easy to decrease the harmonic distortions of AC outputs, thus other circuits are employed so as to gain the better characteristics of the PWM controlling method yet the complexity of the circuit configuration is increased accordingly.

[0006]   Furthermore, a DC/AC inverter with outputs of any kind of waveforms might be the demands in the future so as to cope with the progress of the advanced technologies. Actually, a DC/AC inverter with the programmable output waveforms and frequencies could not be realized by the previously proposed PWM strategies.

[0007]   Keep the drawbacks of the prior arts in mind, and employ experiments and research full-heartily and persistently, the sigma-delta modulation inverter with programmable waveform output is finally conceived by the applicants.

SUMMARY OF THE INVENTION

[0008]   It is therefore an object of the present invention to provide a sigma-delta modulation (SDM) DC/AC inverter with programmable waveform output for simplifying the circuit configuration, decreasing the total harmonic distortion (THD), and increasing the power efficiency.

[0009]   According to the aspect of the present invention, the inverter for converting a DC input voltage into an AC output voltage using the sigma-delta modulation includes: a sigma-delta modulation (SDM) controller for producing a modulated output voltage signal according to a reference voltage signal, a driving circuit electrically connected to the SDM controller for producing a driving signal according to the modulated output voltage signal, and a power inversion stage circuit electrically connected to the driving circuit for producing the AC output voltage according to the driving signal.

[0010]   Preferably, the SDM controller includes: an integrator circuit for producing an integrator output signal according to a difference between the reference voltage signal and the modulated output voltage signal, a sample-and-hold circuit electrically connected to the integrator circuit for sampling and holding the integrator output signal, and a quantizer circuit electrically connected to the sample-and-hold circuit and electrically connected to an input terminal of the integrator circuit

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through an output terminal thereof for quantizing the integrator output signal and producing the modulated output voltage signal.

[0011]   Preferably, the integrator circuit is an integrator.

[0012]   Preferably, the integrator is a differential integrator.

[0013]   Preferably, the sample-and-hold circuit is a sample-and-hold device and is controlled by an external sampling signal.

[0014]   Preferably, the quantizer circuit is a two-level quantizer.

[0015]   Preferably, the two-level quantizer is a two-level comparator.

[0016]   Preferably, the modulated output voltage signal is a pulse train.

[0017]   Preferably, the reference voltage signal is input from an external signal generator.

[0018]   Preferably, the driving circuit is a high/low side driver.

[0019]   Preferably, the power inversion stage circuit includes: a power stage circuit electrically connected to the driving circuit for producing a AC power signal according to the driving signal and the DC input voltage, and a filter circuit electrically connected to the power stage circuit for producing the AC output voltage according to the AC power signal.

[0020]   Preferably, the power stage circuit is in a full-bridge configuration.

[0021]   Preferably, the full-bridge configuration is a H-diagonal structure having four power switches.

[0022]   Preferably, each of the four power switches is a MOSFET.

[0023]   Preferably, the filter circuit is a low-pass filter.

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[0024]   Preferably, the filter circuit comprises an inductor and a capacitor in series.

[0025]   According to another aspect of the present invention, a controller for producing a modulated output voltage signal according to a reference voltage signal includes: an integrator circuit for producing an integrator output signal according to a difference between the reference voltage signal and the modulated output voltage signal, a sample-and-hold circuit electrically connected to the integrator circuit for sampling and holding the integrator output signal, and a quantizer circuit electrically connected to the sample-and-hold circuit and electrically connected to an input terminal of the integrator circuit through an output terminal thereof for quantizing the integrator output signal and producing the modulated output voltage signal.

[0026]   Preferably, the integrator circuit is an integrator.

[0027]   Preferably, the integrator is a differential integrator.

[0028]   Preferably, the sample-and-hold circuit is a sample-and-hold device and is controlled by an external sampling signal.

[0029]   Preferably, the quantizer circuit is a two-level quantizer.

[0030]   Preferably, the two-level quantizer is a two-level comparator.

[0031]   Preferably, the modulated output voltage signal is a pulse train.

[0032]   Preferably, the reference voltage signal is input from an external signal generator.

[0033]   Preferably, the controller is a SDM controller.

[0034]   The present invention may best be understood through the following descriptions with reference to the accompanying drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

[0035]   FIG. 1 is the block diagram of the first preferred embodiment of the SDM DC/AC inverter of the present invention;

[0036]   FIG. 2 is the block diagram of the first preferred embodiment of the SDM controller of the present invention;

[0037]   FIG.s 3(a) and 3(b) are the schematic diagrams showing the waveforms of the reference voltage signal, the output of the integrator circuit, the hold signal, and output of the SDM controller of the present invention when the reference voltage signals are in the positive-half period and in the negative-half period of a sinusoidal waveform respectively;

[0038]   FIG. 4 is the block diagram of the open-looped SDM DC/AC inverter with full-bridge configuration of the present invention;

[0039]   FIG. 5 is the schematic diagram showing the open-looped output-to-control frequency response for the SDM DC/AC inverter of the present invention;

[0040]   FIGs. 6 (a1) and (a2) are the schematic diagrams showing the simulated and measured output waveforms of the present invention respectively when the output power = 1 kVA, the desired output voltage Vout = 110 Vrms, the input waveforms are sinusoidal waveforms, and the frequency of the input waveforms = 1 kHz;

[0041]   FIGs. 6 (b1) and (b2) are the schematic diagrams showing the simulated and measured output waveforms of the present invention

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respectively when the output power = 1 kVA, the desired output voltage Vout = 110 Vrms, the input waveforms are triangular waveforms, and the frequency of the input waveforms = 1 kHz;

[0042]   FIGs. 7 (a1) and (a2) are the schematic diagrams showing the simulated and measured output waveforms of the present invention respectively when the output power = 1 kVA, the desired output voltage Vout = 110 Vrms, the input waveforms are sinusoidal waveforms, and the frequency of the input waveforms = 500 Hz;

[0043]   FIGs. 7 (b1) and (b2) are the schematic diagrams showing the simulated and measured output waveforms of the present invention respectively when the output power = 1 kVA, the desired output voltage Vout = 110 Vrms, the input waveforms are triangular waveforms, and the frequency of the input waveforms = 500 Hz;

[0044]   FIGs. 8 (a1) and (a2) are the schematic diagrams showing the simulated and measured output waveforms of the present invention respectively when the output power = 1 kVA, the desired output voltage Vout = 110 Vrms, the input waveforms are sinusoidal waveforms, and the frequency of the input waveforms = 60 Hz;

[0045]   FIGs. 8 (b1) and (b2) are the schematic diagrams showing the simulated and measured output waveforms of the present invention respectively when the output power = 1 kVA, the desired output voltage Vout = 110 Vrms, the input waveforms are triangular waveforms, and the frequency of the input waveforms = 60 Hz;

[0046]   FIGs. 9 (a1) and (a2) are the schematic diagrams showing the simulated and measured output waveforms of the present invention respectively when the output power = 200 VA, the desired output voltage

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Vout = 110 Vrms, the input waveforms are sinusoidal waveforms, and the frequency of the input waveforms = 1 kHz;

[0047]   FIGs. 9 (b1) and (b2) are the schematic diagrams showing the simulated and measured output waveforms of the present invention respectively when the output power = 200 VA, the desired output voltage Vout = 110 Vrms, the input waveforms are triangular waveforms, and the frequency of the input waveforms = 1 kHz;

[0048]   FIGs. 10 (a1) and (a2) are the schematic diagrams showing the simulated and measured output waveforms of the present invention respectively when the output power = 200 VA, the desired output voltage Vout = 110 Vrms, the input waveforms are sinusoidal waveforms, and the frequency of the input waveforms = 500 Hz;

[0049]   FIGs. 10 (b1) and (b2) are the schematic diagrams showing the simulated and measured output waveforms of the present invention respectively when the output power = 200 VA, the desired output voltage Vout = 110 Vrms, the input waveforms are triangular waveforms, and the frequency of the input waveforms = 500 Hz;

[0050]   FIGs. 11 (a1) and (a2) are the schematic diagrams showing the simulated and measured output waveforms of the present invention respectively when the output power = 200 VA, the desired output voltage Vout = 110 Vrms, the input waveforms are sinusoidal waveforms, and the frequency of the input waveforms = 60 Hz; and

[0051]   FIGs. 11 (b1) and (b2) are the schematic diagrams showing the simulated and measured output waveforms of the present invention respectively when the output power = 200 VA, the desired output voltage

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Vout = 110 Vrms, the input waveforms are triangular waveforms, and the frequency of the input waveforms = 60 Hz.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0052]   Please refer to FIG. 1, it is the block diagram of the first preferred embodiment of the SDM DC/AC inverter of the present invention including a SDM controller 11, a high/low side driver 12, and a power inversion stage circuit 13 having a power stage circuit 131 and a filter circuit 132.

[0053]   The SDM controller 11 is employed for producing a modulated output voltage signal according to the reference voltage signal. The high/low side driver 12 is electrically connected to the SDM controller 11 for producing a plurality of driving signals according to the modulated output voltage signal.   The power inversion stage circuit 13 is electrically connected to the high/low side driver 12 for producing a AC output voltage $V_o(t)$ according to the controlling of those driving signals and the DC input voltage $V_{dc}(t)$.

[0054]   In the power inversion stage circuit 13, the power stage circuit 131 is employed for producing the power AC signal $V_{AB}(t)$ according to the driving signals and the DC input voltage $V_{dc}(t)$, and a filter circuit 132 is electrically connected to the power stage circuit for producing power AC output voltage $V_o(t)$ according to the power AC signal $V_{AB}(t)$.   The full-bridge configuration is employed by the power stage circuit 13, in which, the switches (Q1, Q4) and (Q2, Q3) are switched in pairs, and the two pairs are in reverse phases so as to offer a higher power output and to minimize the sizes of the elements of output filter using high-frequency switching techniques.   At the output stage, a

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second-order low-pass filter is formed by a L-C configuration to filter the high frequency signal, to modify the output voltage waveforms, and to offer the power source voltage needed by the load R. Since the full-bridge configuration is employed, the modulated output signals of the SDM controller 11 can not be used to drive the four sets of the switches (Q1, Q2, Q3, Q4) of the power stage circuit 131 directly especially for the upper two switches (Q1, Q3) of the left and right arms. Therefore, the high/low side driver 12 is employed in the present invention so as to gain better driving signals.

[0055]   As for the controlling stage portion, the SDM technique is employed to control the shapes of the output voltages, which is the main feature of the present invention. According to the circuitry in FIG. 1, when the Q1 and Q4 are on and Q2 and Q3 are off, the dynamic equations of the state-space can be expressed as follows:

$$\begin{bmatrix} \dfrac{di_L(t)}{dt} \\ \dfrac{dv_c(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} V_{dc} \qquad (1)$$

$$v_o(t) = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} \qquad (2)$$

[0056]   When the Q1 and Q4 are off and Q2 and Q3 are on, the dynamic equations of the state-space can be expressed as follows:

$$\begin{bmatrix} \dfrac{di_L(t)}{dt} \\ \dfrac{dv_c(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + \begin{bmatrix} -\dfrac{1}{L} \\ 0 \end{bmatrix} V_{dc} \qquad (3)$$

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$$v_o(t) = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} \tag{4}$$

According to the state-space averaging technique, the dynamic equations of the state-space can be modified as follows:

$$\begin{bmatrix} \dfrac{di_L(t)}{dt} \\ \dfrac{dv_c(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + \begin{bmatrix} \dfrac{2d-1}{L} \\ 0 \end{bmatrix} V_{dc} \tag{5}$$

$$v_o(t) = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} \tag{6}$$

[0057]   Therein, the d is the duty cycle of the Q1 and Q4.   If the perturbations are $\tilde{i}_L(t)$ ' $\tilde{v}_c(t)$ ' $\tilde{v}_o(t)$ ' $\tilde{d}(t)$ and $\tilde{v}_{dc}(t)$, they can be expressed as follows:

$$i_L(t) = I_L + \tilde{i}_L(t) \tag{7}$$

$$v_c(t) = V_c + \tilde{v}_c(t) \tag{8}$$

$$v_o(t) = V_o + \tilde{v}_o(t) \tag{9}$$

$$d(t) = D + \tilde{d}(t) \tag{10}$$

$$v_{dc}(t) = V_{dc} + \tilde{v}_{dc}(t) \tag{11}$$

[0058]   Assume that $\tilde{v}_{dc}(t) = 0$ to simplify the analysis, then we have:

$$v_{dc}(t) = V_{dc} \tag{12}$$

[0059]   Substitute (7) to (12) into (5) and (6), we get:

$$\begin{bmatrix} \dfrac{d\tilde{i}_L(t)}{dt} \\ \dfrac{d\tilde{v}_c(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{RC} \end{bmatrix} \begin{bmatrix} \tilde{i}_L(t) \\ \tilde{v}_c(t) \end{bmatrix} + \begin{bmatrix} \dfrac{2V_{dc}}{L} \\ 0 \end{bmatrix} \tilde{d}(t) \tag{13}$$

$$\tilde{v}_o(t) = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} \tilde{i}_L(t) \\ \tilde{v}_c(t) \end{bmatrix}$$ (14)

[0060] The steady-state equations are as follows:

$$\begin{bmatrix} 0 & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{RC} \end{bmatrix} \begin{bmatrix} I_L \\ V_c \end{bmatrix} + \begin{bmatrix} \dfrac{2D-1}{L} \\ 0 \end{bmatrix} V_{dc} = 0$$ (15)

$$V_o(t) = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} I_L \\ V_c \end{bmatrix}$$ (16)

[0061] From (15) and (16), the voltage transfer characteristics under the steady-state can be expressed as follows:

$$\frac{V_o}{V_{dc}} = 2D - 1$$ (17)

[0062] By taking the Laplace Transform of (13) and (14), the power stage transfer function can be expressed as follows:

$$G_p(s) \equiv \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{\dfrac{2V_{dc}}{LC}}{s^2 + \dfrac{1}{RC}s + \dfrac{1}{LC}}$$ (18)

[0063] Please refer to FIG. 2, it is the block diagram of the first preferred embodiment of the SDM controller of the present invention including a integrator circuit 111, a sample-and-hold circuit 112, and a quantizer circuit 113. Therein, the integrator circuit 111 is a differential integrator, the quantizer circuit 113 is a two-level quantizer, and the sample-and-hold circuit 112 is a sample-and-hold device and is controlled by an external sampling signal. The circuitry configuration showing in FIG. 2 is a first-order SDM controller, in which the SDM controller 11 can be referred to as a kind of pulse density modulation (PDM) controller so as to transfer the reference voltage signal into a modulated output

voltage signal (a series of pulse signals/a pulse train). The frequency of the pulse signals is decided by the frequency of sampling. If the reference voltage signal has a higher voltage level, the output pulses will have a higher density. If the reference voltage signal has a lower voltage level, the output pulses will have a lower density.

[0064]   The main principle of the above-mentioned SDM controller 11 is to input the reference voltage signal and to compare it with the initial output value of the SDM controller to produce an error signal which will be integrated by the integrator circuit 111, be proceeded through a high-frequency sampling-and-holding by the sample-and-hold circuit 112, and be quantized by the quantizer circuit 113 lastly. In general, a two-level comparator is employed as the two-level quantizer 113 to quantize the output (to modulate the output voltage signal) and to feedback to the input of the controller 11 so as to compare with the reference voltage signal again. Through this repetitive action, a series of pulse signals will be produced at the output terminal of the quantizer circuit 113, which is also the output terminal of the SDM controller 11, to drive the switch elements (Q1, Q2, Q3, Q4) of the power inversion circuit 13 to control the power outputs and the output waveforms. According to the feedback control theory, if the gain of the loop is large enough, the average value of the modulated output voltage signals will approach the average value of the reference voltage signals.

[0065]   Referring to FIG. 2, the relationships between the SDM loop signals can be defined as follows:

$$v_{int}(t) = \frac{1}{R_{int}C_{int}} \int \left[v_r(t) - v_q(t) \right] dt \qquad (19)$$

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$$v_h(t) = \sum_{i=1}^{\infty} \sum_{j=0}^{N_t} v_{int}(jT_c)\left[u(t - t_{i,0} - jT_c) - u(t - t_{i,0} - (j+1)T_c)\right] \qquad (20)$$

$$v_q(t) = V_q sgn(v_h(t)) = \begin{cases} +V_{cc}, & v_h(t) \geq 0 \\ -V_{cc}, & v_h(t) < 0 \end{cases} \qquad (21)$$

[0066]   Considering that the reference voltage signal is a sinusoidal signal, the reference voltage signal is defined as follows:

$$v_r(t) = V_{rm} \sin \omega t \qquad (22)$$

[0067]   In which, the V_{rm} is the peak value of the reference voltage signal, and ω is the angle frequency of the reference voltage signal. In order to avoid an over-modulated phenomenon which will cause a higher distortion problem, assume that $V_{rm} < V_{cc}$. Please refer to FIG. 3, when $t = t_{i,0}$ and $v_q(t_{i,0}) = -V_{cc}$, the relationships between the SDM loop signals can be defined as follows:

$$v_{int}(t_{i,1}) = \frac{1}{R_{int}C_{int}} \int_{t_{i,0}}^{t_{i,1}} \left[v_r(t) - v_q(t)\right]dt + v_{int}(t_{i,0})$$

$$= \frac{1}{R_{int}C_{int}}\left[-\frac{V_{rm}}{\omega}(\cos\omega\, t_{i,1} - \cos\omega\, t_{i,0}) + V_{cc}(t_{i,1} - t_{i,0})\right] + v_{int}(t_{i,0}) \qquad (23)$$

$$v_h(t_{i,1}) = v_{int}(t_{i,1}) > 0 \qquad (24)$$

$$v_q(t_{i,1}) = +V_{cc} \qquad (25)$$

[0068]   Since the modulated output voltage is subtracted from the reference input voltage and the result is a positive value, the slope of the integrated output of the integrator circuit 111 is positive. Considering that the sampling frequency is far greater than the reference voltage signal frequency, the reference voltage signal can be considered as a constant value during the sampling period. Assuming that $m = \dfrac{v_r}{V_{cc}}$ and $K = \dfrac{1}{R_{int}C_{int}}$, the integrated output slope of the integrator circuit 111 is

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$K(m+1)V_{cc}$. After sampling and holding, the result is larger than zero and the modulated output will be changed from $-V_{cc} \rightarrow +V_{cc}$.

$$v_{int}(t_{i,2}) = \frac{1}{R_{int}C_{int}} \int_{t_{i,1}}^{t_{i,2}} \left[v_r(t) - v_q(t) \right] dt + v_{int}(t_{i,1})$$

$$= \frac{1}{R_{int}C_{int}} \left[-\frac{V_{rm}}{\omega}(\cos\omega\, t_{i,2} - \cos\omega\, t_{i,1}) - V_{cc}(t_{i,2} - t_{i,1}) \right] + v_{int}(t_{i,1}) \qquad (26)$$

$$v_h(t_{i,2}) = v_{int}(t_{i,2}) > 0 \qquad (27)$$

$$v_q(t_{i,2}) = +V_{cc} \qquad (28)$$

[0069] Since the modulated output voltage is subtracted from the reference input voltage and the result is a negative value, the slope of the integrated output of the integrator circuit 111 is negative and will have a value of $K(m-1)V_{cc}$. After sampling and holding, the result is still greater than zero and the modulated output will be kept $+V_{cc}$. The motions of the SDM controller is as so, after n times of sampling and holding, the result is smaller than zero, and the modulated output is changed from $-V_{cc} \rightarrow +V_{cc}$ so as to finish a switching period.

[0070] Please refer to FIGs. 3(a) and 3(b), which are the schematic diagrams showing the waveforms of the reference voltage signal, the output of the integrator circuit, the hold signal, and output of the SDM controller of the present invention when the reference voltage signals are in the positive-half period and in the negative-half period of a sinusoidal waveform respectively. Referring to FIG. 3, the duty cycle of the modulated voltage signal is increased as the reference voltage signal is increased. Assuming that the sampling frequency is far greater than the reference voltage signal frequency, the variations of reference voltage

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signal is quite small and can be considered as a constant value thus the increased variation amount and the decreased variation amount of the output of integrator circuit 111 during the period of sampling are the same, and:

$$K(m+1)V_{cc} = -nK(m-1)V_{cc} \qquad (29)$$

[0071]   From (29), we have:

$$n = \frac{1+m}{1-m} \qquad (30)$$

[0072]   If d is the duty cycle of the output modulated voltage signal, we get:

$$d = \frac{n}{1+n} = \frac{1+m}{2} \qquad (31)$$

$$d(t) = \frac{1}{2} + \frac{v_r(t)}{2V_{cc}} \qquad (32)$$

, and $0 < d(t) < 1$.

[0073]   Please refer to FIG. 4, it is the block diagram of the open-looped SDM DC/AC inverter with full-bridge configuration of the present invention.   Considering that the reference voltage signal of the SDM controller 41, $v_r(t)$, has a perturbation $\tilde{v}_r(t)$, we have:

$$v_r(t) = V_r + \tilde{v}_r(t) \qquad (33)$$

[0074]   Substitute (10) and (33) into (32), we get:

$$\tilde{d}(t) = \frac{\tilde{v}_r(t)}{2V_{cc}} \qquad (34)$$

$$D = \frac{1}{2} + \frac{V_r}{2V_{cc}} \qquad (35)$$

[0075]   By taking the Laplace Transform of (34), the modulation transfer function $G_m(s)$ can be expressed as follows:

$$G_m(s) \equiv \frac{\tilde{d}(s)}{\tilde{v}_r(s)} = \frac{1}{2V_{cc}} \qquad (36)$$

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[0076]   The power stage transfer function of the power inversion stage circuit 42, $G_p(s)$, is defined in (18). From (18) and (36), the transfer function of the modulated output voltage signal and the reference voltage signal, $G_1(s)$, can be expressed as follows:

$$G_1(s) \equiv \frac{\tilde{v}_o(s)}{\tilde{d}(s)} \frac{\tilde{d}(s)}{\tilde{v}_r(s)} = \frac{V_{dc}}{V_{cc}} \frac{\frac{1}{LC}}{s^2 + \frac{1}{RC}s + \frac{1}{LC}} \qquad (37)$$

RESULTS OF SIMULATION AND MEASUREMENT

[0077]   A full-bridge configuration is employed in the DC/AC inverter of the present invention, a first-order SDM controller is used to modulate the high/low of the output voltage and the waveforms, and through the low-pass filter to filter the high-frequency harmonic waves so as to have a smooth voltage waveforms.   According to the above-mentioned theory, the simulations and measurements of a 1 kVA DC/AC inverter circuit of the present invention have been accomplished. The DC input voltage is 200V, the AC output voltage is 110V, the capacitance of the output LC filter is $C = 0.22\mu F$, the inductance of the output LC filter is $L = 1mH$, the cutoff frequency of the output LC filter is 10.7kHz.   The open-loop output-to-control frequency responses for the provided SDM DC/AC inverter are simulated, and the results of simulation are shown in FIG. 5, in which the phase margin is 65° and the gain margin is 60 dB.

[0078]   When the output power is 1 kVA, the desired output voltage is 110 Vrms, and the input frequencies are 1kHz, 500Hz, and 60Hz respectively, the simulated waveforms using the Is Spice simulation

software to simulate the sinusoidal and triangular waves and the measured output waveforms of the present invention are shown in FIG. 6(a1) to FIG. 8(b2), in which the power efficiency is up to 92% and the total harmonic distortion (THD) is less than 1.652%.

[0079]   When the output power is 200VA, the desired output voltage is 110 Vrms, and the input frequencies are 1kHz, 500Hz, and 60Hz respectively, the simulated waveforms using the Is Spice simulation software to simulate the sinusoidal and triangular waves and the measured output waveforms of the present invention are shown in FIG. 9(a1) to FIG. 11(b2), in which the power efficiency is up to 83% and the total harmonic distortion (THD) is less than 1.733%. The measured output power, frequencies, output voltages, THDs, and the power efficiencies of the provided circuit of the present invention are shown in table 1.

Table 1

Output power (VA)	Frequency (Hz)	$V_{o,rms}$ (V)	THD (%)	Power efficiency (%)
200	60	110	1.078	88
	500	110	1.488	85
	1k	110	1.733	83
1k	60	110	0.998	94
	500	110	1.066	93
	1k	110	1.652	92

[0080]   In conclusion, the present invention applied the SDM technique to a DC/AC inverter, a SDM controller is used to modulate a reference voltage signal to a series of pulse signals, to amplify the signal

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power through a power inversion stage circuit, and to restore the signal waveforms through the filter circuit so as to simplify the circuitry configuration, to decrease the THD, and to output any kind of waveforms thus achieving the improvement of the drawbacks of the prior art.

[0081]   Although the present invention has been described and illustrated in an example of the most preferred embodiment, the constructional characteristics of the present invention are not limited by that.   The variations and modifications that anyone who is familiar with the skill can think of easily which fall within the spirit and scope of the present invention as defined by the appended claims should be included.